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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/768,121	01/23/2001	Frank O. Distler	BUR920000123USI	3330

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EXAMINER
WHITTINGTON, ANTHONY T

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 06/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/768,121	DISTLER ET AL.	
	Examiner	Art Unit	
	Anthony T Whittington	2133	

-- The MAILING DATE of this communication appears on the cover she t with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 March 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 4,20,23 and 24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 4 and 20, the phrase "a **substantial** portion" renders the claim indefinite because it is unclear to the Examiner how large or small the number of care bits need to be XORed in the test vector. The Examiner would appreciate if the Applicants would clarify this matter.

Regarding claims 23 and 24, the phrase " **sufficient** to raise the fault coverage" renders the claim indefinite because it is unclear to the Examiner what threshold value is sufficient to raise the fault coverage. The Examiner would appreciate if the Applicants would clarify this matter.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

Rejection under 35 U.S.C. 102(e), Patent to Another with Earlier Filing Date, Reference is a U.S. Patent Issued Directly or Indirectly From a National Stage of, or a Continuing Application Claiming benefit under 35 U.S.C. 365(c) to, an International Application Having an International Filing Date Prior to November 29, 2000

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims1-3, 5-19, 21 and 22 are rejected under 35 U.S.C. 102(e) as being anticipated by Rajski et al. (U.S. 6,327,687).

As per claim 1, Rajski et al. teaches a method for reducing test data volume in the testing of logic products comprising all the steps of the instant application. Rajski et al. teaches generating an original test vector in column 5, lines 6-7, which state: "the ATPG tool generates test vectors". Rajski et al. teaches filling non-care bits with a repeated value to form a highly compressible test vector data set in column 8, lines 57-60: "The remaining scan cells that are 'don't cares'...in the compressed test pattern and are filled with a pseudo-random values generated"(filling non-care bits with a repeated value to form a highly compressible test vector data set). Rajski et al. teaches compressing the test vector data set to form compressed test vector in column 4, lines 55-57: "A method ...is used to generate a compressed test pattern".

As per claim 2, Rajski et al. teaches transmitting the compressed test data to a test system and recovering the care bits for loading into input latches of a tester in column 4 lines 57-60:

"The compressed test pattern is stored in an ATE and is applied on input channels to an integrated circuit being tested."

As per claims 3 and 18, Rajski et al. teaches generating a background vector data set (generate a test cube, 62) in Figure 5. Rajski et al. teaches forming a differential vector data set by XORing care bits with background vector bits in Figure 7.

As per claims 4 and 20, Rajski et al. teaches XORing sets a substantial portion of the care bits to a value 0 in Table 8(column 13, lines 44-59).

As per claim 5, Rajski et al. teaches an algorithm (Gauss-Jordan elimination) used in header identification and a seed used to generate vector data in column 10,line 65 through column 11, line 20: " Gauss-Jordan techniques...It can be verified...resulting seed variables".

As per claim 6, Rajski et al. teaches decompressing the compressed test vector data (decompressor, 36) in Figure 2. Rajski et al. teaches extracting and reconstructing vector data in Figure 4. Rajski teaches XORing the reconstructed background vector data to form a reconstructed test vector data in Figure 7.

As per claims 7 and 10, Rajski et al. teaches reconstructed test data vectors with care bits and non-care bits in Figure 8.

As per claims 8 and 19, Rajski et al. teaches a random distribution of bits having both "0" and "1" in column 3,lines 10-11: "Weighted random patterns have been primarily used".

As per claims 9 and 15, Rajski et al. teaches a method for reducing test data volume in the testing of logic products comprising all the steps of the instant application. Rajski et al. teaches generating redundant test vectors in column 5, lines 6-7, which states: "the ATPG tool generates test vectors". Rajski et al. teaches utilizing a repeat capability of a tester to load input

latches of the tester in column 4 lines 57-60: "The compressed test pattern is stored in an ATE and is applied on input channels to an integrated circuit being tested."

As per claims 11,12 and 16, Rajski et al. teaches a test vector data that comprises a matrix of test vectors arranged in rows and columns in Table 2(column 10, lines 46-56). Rajski et al. teaches a different care bit is repeated in the same column for each row of the matrix in Table 4(column 11, lines 24-34).

As per claim 13, Rajski teaches a computer-usable medium storing computer-executable instructions volume in the testing of logic products comprising all the steps of the instant application. Rajski et al. teaches generating an original test vector in column 5, lines 6-7, which state: "the ATPG tool generates test vectors". Rajski et al. teaches filling non-care bits with a repeated value to form a highly compressible test vector data set in column 8, lines 57-60: "The remaining scan cells that are 'don't cares'...in the compressed test pattern and are filled with a pseudo-random values generated"(filling non-care bits with a repeated value to form a highly compressible test vector data set). Rajski et al. teaches compressing the test vector data set to form compressed test vector in column 4, lines 55-57: "A method ...is used to generate a compressed test pattern".

As per claim 14, Rajski teaches a computer-usable medium storing computer-executable instructions volume in the testing of logic products comprising all the steps of the instant application. Rajski et al. teaches transmitting the compressed test data to a test system and recovering the care bits for loading into input latches of a tester in column 4 lines 57-60: "The compressed test pattern is stored in an ATE and is applied on input channels to an integrated circuit being tested."

As per claims 17, Rajski teaches a method comprising all the elements of the instant application. Rajski teaches forming a compressed test data by setting a care bits and non-care bits in Figure 8. Rajski et al. teaches a downloading a test data into a testing system and loading input latches in column 4 lines 57-60: "The compressed test pattern is stored in an ATE and is applied on input channels to an integrated circuit being tested." Rajski et al. teaches decompressing the compressed test vector data (decompressor, 36) in Figure 2.

As per claim 21, Rajski et al. teaches a method for testing logic products comprising all the elements of the instant application. Rajski et al. teaches a first testing technique that loads input latches of a tester in column 4 lines 57-60: "The compressed test pattern is stored in an ATE and is applied on input channels to an integrated circuit being tested." Rajski et al. teaches a second technique that loads input latches by repeating test vector of a minimum set of test vectors obtained by repeating a last care bit in neighboring non-care bit in Figures 10 and 11.

As per claim 22, Rajski et al. teaches ranges of fault coverage that covers all the ranges in the instant application in column 2, lines 23-41.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patents are cited to further show the state of art with respect to test vector compression in general:

U.S. Pat No. 5,991,909 to Rajski et al.

U.S. Pat No. 6,557,129 to Rajski et al.

U.S. Pat No. 5,485,471 to Bershteyn

U.S. Pat No. 5,416,783 to Broseghini et al.

U.S. Pat No. 5,719,881 to Yonetoku

U.S. Pat No. 6,334,199 to Ono et al.

U.S. Pat No. 6,202,187 to Akiyama

U.S. Pat No. 6,061,818 to Touba et al.

U.S. Pat No. 6,401,226 to Maeno

U.S. Pat No. 6,427,218 to Takeoka

U.S. Pat No. 6,449,743 to Hosokawa

U.S. Pat No. 5,883,906 to Turnquist et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anthony T Whittington whose telephone number is 703-306-5617. The examiner can normally be reached on Monday-Friday 7:30a.m.-4:00p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 703-305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

A.W.
May 29, 2003

EMMANUEL L. MOISE
PRIMARY EXAMINER
A/U 2133